

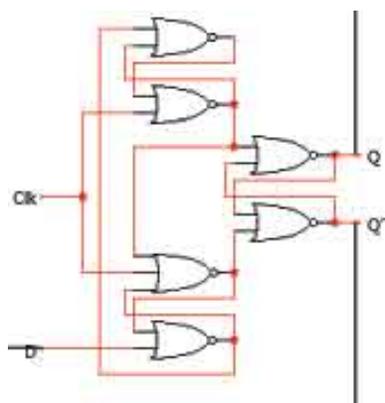
CS 150, Fall 2001
Midterm #1
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Problem #1

You are given a negative edge triggered D flip-flop as shown on page 1-19 of the notes on sequential logic.

a) Design the combinational logic necessary to convert this flip-flop into a negative edge-triggered J-K flip-flop. Leave your solution in sum-of-products form. Write out the equation for the combinational logic block, and draw the block connected to the FF below.

Equation:

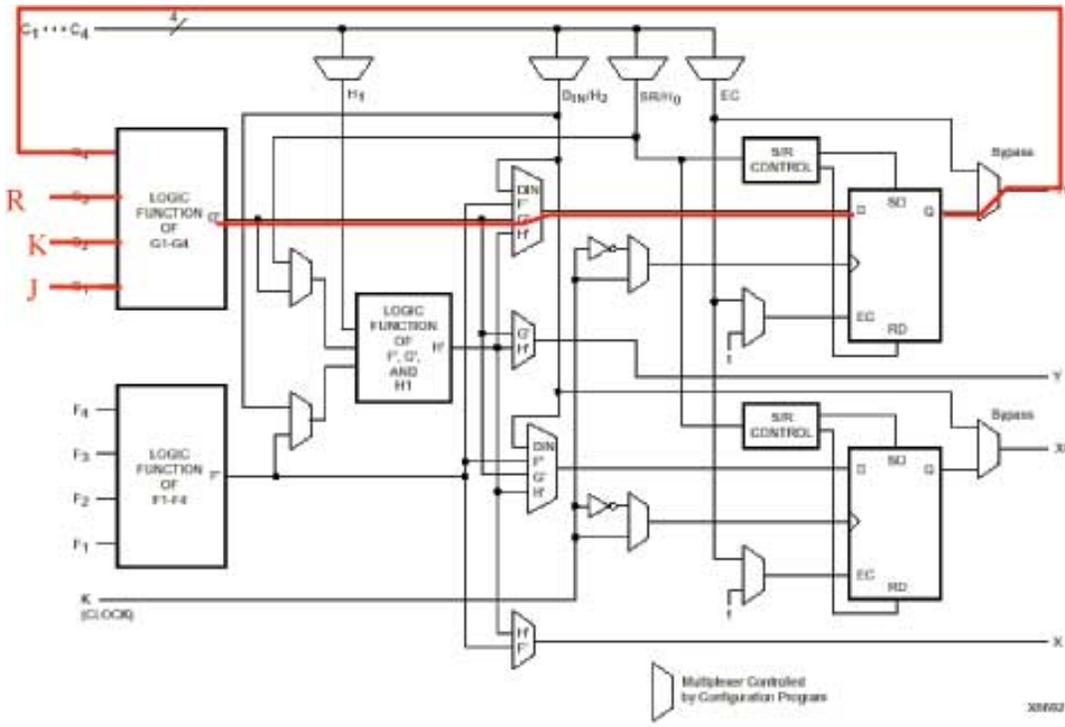


b) Assume the setup and hold times for the D-FF above are 20ns and 10ns respectively. What is the minimum propagation delay for the D-FF for it to meet correct timing criteria? Why?

c) Suppose the propagation delay for the D-FF is 20ns and the clock frequency is 10 MHz. What is the maximum delay per gate allowed in the sum-of-products combinational logic block that you designed? Give a reason for your answer, and show your calculations. Assume that all gates in your combination block have identical delay. Also assume that J' and K' are available for free (i.e., no delay in inverting the J and K signals).

d) Recalculate the SOP equation describing the combinational logic block assuming that you must now also implement a synchronous reset signal.

e) Suppose you are to implement the J-K flip-flop with synchronous reset from above in a Xilinx CLB. Mark the active blocks and multiplexer paths on the diagram below.



f) How many J-K FF's can be implemented per CLB?

g) Suppose you wanted to implement a J-K FF with synchronous set and reset using a full SOP form. Now, how many J-K FFs can be implemented per CLB?

Problem #2

You are implementing the brains for a "smart" washing machine. The washing machine works in the following manner:

- When you press "Start" after loading in the clothes, the washing machine determines the load size (Medium / Large) and then dispenses the appropriate amount of water and detergent.
- The machine then washes the clothes for 10 minutes.
- The machine then rinses the clothes for 10 minutes. If the effluent is dirty at the end of the rinse, the machine repeats the dispense, wash + rinse cycle, but for no more than a total of 3 cycles.
- The machine then spin-dries the clothes until it detects no water discharge, but for not more than 20 minutes.

Inputs:

- START Button
- MEDIUM load sensor
- LARGE load sensor
- DIRTY effluent sensor
- WET water discharge sensor
- T1DONE = 60 min timer
- T2DONE = 10 min timer

Outputs:

- MEDIUM water + soap dispense
- LARGE water + soap dispense
- WASH cycle actuator
- RINSE cycle actuator
- DRY cycle actuator
- T1START 60 min timer start
- T2START 10 min timer start

Draw a Mealy machine FSM for this system.

Problem #3

ASCII, as you know, is a common data representation format. Write the state transition table for an ASCII hexadecimal counter; i.e., a counter that counts from 0-15 and outputs the results as 0-9, A-F in ASCII (NOTE: Characters 0-9 are 48-57 in base 10 ASCII; characters A-F are 65-70 in base 10 ASCII). Assume the data is stored in an 8-bit wide D-FF register.

Current State										Next State									
Base10	Hex	Register Contents								Base10	Hex	Register Contents							
		Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1			N8	N7	N6	N5	N4	N3	N2	N1
0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	1
1	1	0	0	1	1	0	0	0	1	2	2	0	0	1	1	0	0	1	0
2	2	0	0	1	1	0	0	1	0	3	3	0	0	1	1	0	0	1	1
3	3	0	0	1	1	0	0	1	1	4	4	0	0	1	1	0	1	0	0
4	4	0	0	1	1	0	1	0	0	5	5	0	0	1	1	0	1	0	1
5	5	0	0	1	1	0	1	0	1	6	6	0	0	1	1	0	1	1	0
6	6	0	0	1	1	0	1	1	0	7	7	0	0	1	1	0	1	1	1
7	7	0	0	1	1	0	1	1	1	8	8	0	0	1	1	1	0	0	0
8	8	0	0	1	1	1	0	0	0	9	9	0	0	1	1	1	0	0	1
9	9	0	0	1	1	1	0	0	1	10	A	0	1	0	0	0	0	0	1
10	A	0	1	0	0	0	0	0	1	11	B	0	1	0	0	0	0	1	0
11	B	0	1	0	0	0	0	1	0	12	C	0	1	0	0	0	0	1	1
12	C	0	1	0	0	0	0	1	1	13	D	0	1	0	0	0	1	0	0
13	D	0	1	0	0	0	1	0	0	14	E	0	1	0	0	0	1	0	1
14	E	0	1	0	0	0	1	0	1	15	F	0	1	0	0	0	1	1	0
15	F	0	1	0	0	0	1	1	0	16	0	0	0	1	1	0	0	0	0

a) Determine the next state functions for N8 and N7 in abbreviated SOP form:

b) Simply N7 to its simplest form, and draw the combinational logic block as it would connect to the D input of FF7.

c) What is the minimum # of FFs you would need to implement the counter in the following schemes? Give reasons for your answers.

i) One-hot

ii) Sequential

Problem #4

You are to implement a 2-bit shift register using D-FFs with some special features. The register has 3 modes of operation determined by two input bit (C1) - 00, 01, 10, 11.

- 1) 00: The shift register right shifts, taking input from LIN \rightarrow Q2 \rightarrow Q1
- 2) 01: The shift register left shifts, taking input from RIN \rightarrow Q1 \rightarrow Q2
- 3) 10: The shift register loops back, i.e., Q2 \rightarrow Q1, Q1 \rightarrow Q2
- 4) 11: The shift register toggles all its bits, i.e., all ones become zeroes and vice versa

Draw the FSM diagram for this shift register.

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**If you have any questions about these online exams
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