Your Name: _____

UNIVERSITY OF CALIFORNIA AT BERKELEY

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Department of Electrical Engineering and Computer Sciences

CS 150 - Spring 1997
Prof. A. R. Newton

(1)	/20
(2)	/20
(3)	/20
(4)	/20
(5)	/20
TOTAL	**/100**

Final Examination

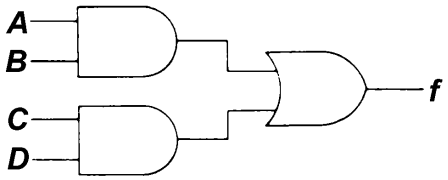
(Open Katz, Calculators OK, 3 hours)

Include all final answers in locations indicated on these pages. Use space provided for all working. If necessary, attach additional sheets by staple at the end. State all assumptions made.

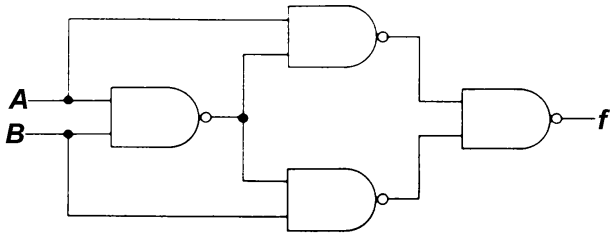
BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) (20pts)

(a) Realize the following circuit using **OR gates in the first stage and AND gates in the second stage**. **Do not use any other gates** (no inverters) and **assume complements are not available**.



(b) Write the output *f* of the circuit shown below in terms of *A* and *B* in as compact a form as possible.

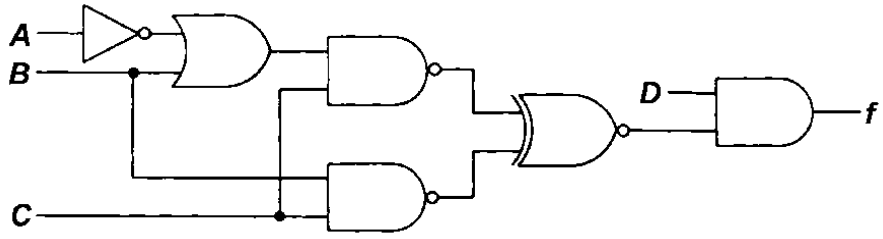


1(a) (5pts) Schematic diagram:

1(b) (5pts)

f = _____

1 (c) Reduce the following circuit to obtain the most compact (**minimum number of gates+gate inputs**) form. Use only simple gates (AND, NAND, NOR, OR, inverter, XOR, XNOR).



(d) A four-bit binary number {A,B,C,D}, where A is the most significant digit and D the least significant digit, appears on the input to a combinational logic circuit**. Output X indicates whether the number is divisible by 2** without any remainder and **output Y indicates if the number is divisible by 3** without remainder. **Obtain the sum-of-products logic equations for X and Y with the minimum number of literals.**

1(c) (5pts) Schematic:

1(d) (5pts)

X = _____

Y = _____

Additional Space for Problem 1

CD \ AB	00	01	11	10
00				
01				
11				
10				

CD \ AB	00	01	11	10
00				
01				
11				
10				

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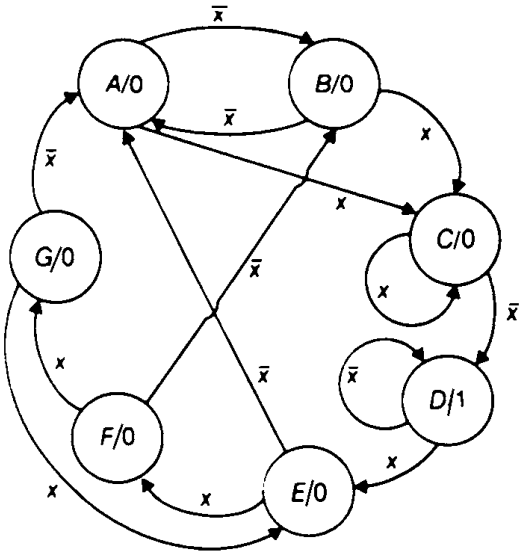
(2) (20pts)

(a) Consider the following state transition graph. Use **an implication table to eliminate any redundant states**. **List all equivalent states**. Show your final result as a **state transition graph**.



2(a) (10pts)
Equivalent states: _____

_____

Reduced STG:

Additional space for problem 2(a)

(b) Consider the following reduced state table. For the **state assignment A={00}, C={01}, D={11} and E = {10}, implement the machine using JK flip-flops and logic gates only**. Show **your flip-flop excitation and output K-maps**, the **flip-flop input excitation equations**, the **output equation**, and a **schematic diagram for the final implementation** using as few simple logic gates as possible.

PS	NS		Z
	$x = 0$	$x = 1$	
A	A	C	0
C	D	C	0
D	D	E	1
E	A	E	0

2(b) (10 pts)

(i) Excitation and output K-maps:

(ii) Flip-flop input excitation equations and output equation:

_____ _____

_____ _____

_____ _____

(iii) Schematic diagram:

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(3) (20pts)
A **one-bit shifter** is defined as follows:

$$y = \begin{cases} x_{-1} & if \quad d = 1, s = 1 \\ x_{+1} & if \quad d = 0, s = 1 \\ x & if \quad s = 0 \end{cases}$$

(a) Obtain an **implementation of the one-bit shifter using a single 4-input, 2 select line MUX only.**
(b) Show how it would be possible to build an ***n*-bit shifter** (shift each bit of an *n*-bit word $\{x_0, x_1, \ldots, x_{n-1}\}$ one bit position up or down) using a number of your one-bit shifters from part (a) above.

3 (a) (5pts) One-bit shifter:

3(b) (5pts) *n*-bit shifter:

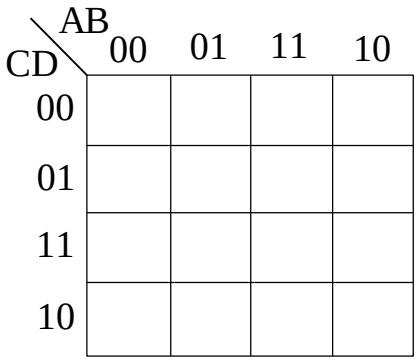
(**3) (continued)** Consider the function: f(A,B,C,D) = $\Sigma m(3,4,8,9,10,13,14,15)$

(c) Implement this function using a single 4-input, 2 select line MUX and as few additional gates as possible. **Assume complements are *not* available.**

(d) Implement the function using a minimum number of 2-input, 1 select line MUX's and a single 4-input, 2 select line MUX only (no additional logic gates). **Assume complements *are* available**.

3(c) (5pts) Schematic:

3(d) (5pts) Schematic:



Your Name: _____

(4) (20pts)

(a) Show a **merger diagram** for the primitive flow table shown at right. Show **the merged flow table** for the design.

X1 X2				Z
00	01	11	10	
(1)	6	5	2	0
1	4	3	(2)	0
8	4	(3)	7	1
8	(4)	3	7	1
1	6	(5)	2	0
1	(6)	5	2	0
8	6	5	(7)	1
(8)	4	5	7	1

4(a) (10pts) Merger Diagram:

Merged flow table:

Additional space for Problem 4(a)

(b) **Obtain a race-free state assignment** for the merged flow table shown below. You are to assign the codes for the two unassigned states and **you may *not* use any additional states** to implement the race-free assignment. Show your solution by filling in all fields (including a glitch-free output assignment for Z) on the empty table shown below.

State Assignments (Q_1Q_2)	AB 00	01	11	10
00	(1)	(7)	8	2
	(3)	(5)	6	4
01	3	7	(8)	(2)
	3	7	(6)	(4)

Merged Flow Table

AB 00	01	11	10
1	0		
0	1		
		1	1
		0	1

Z

4(b) (10pts) Final merged flow table and state assignment:

State Assignments (Q_1Q_2)	AB 00	01	11	10
00	◯	◯		
___	◯	◯		
01			◯	◯
___			◯	◯

Merged Flow Table

AB 00	01	11	10
1	0		
0	1		
		1	1
		0	1

Z

Additional space for Problem 4(b)

Your Name: _____

(5) (a) Design a counter which produces the following binary sequence**: 0, 1, 3, 7, 6, 4 and then repeats**. Use three clocked T flip-flops and logic gates only. Use a minimum number of additional logic gates.

(b) How would you use **a ROM** to perform the **addition of two four-bit 2's-complement numbers**? How many **address lines** would be required? How many **data lines**? Show the **binary values** that would be applied to the address lines and observed on the data lines of the ROM when performing the following computations:

(i) (+1) + (+2) **(ii)** (-1) + (+1) **(iii)** (+7) + (+6) **(iv)** (-6) + (-1)

5(a) (14pts) T flip-flop input equations:

T_1 = _____ **T_2 = _____** **T_3 = _____**

5(b) (6pts)

Address lines: _____ **Data lines: _____**

	ADDRESS BITS	**DATA OUTPUT**
(i)	_____	_____
(ii)	_____	_____
(iii)	_____	_____
(iv)	_____	_____

Additional Space for Problem 5

Additional Space for Working Problems