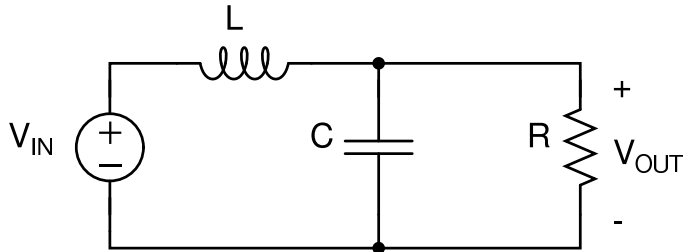


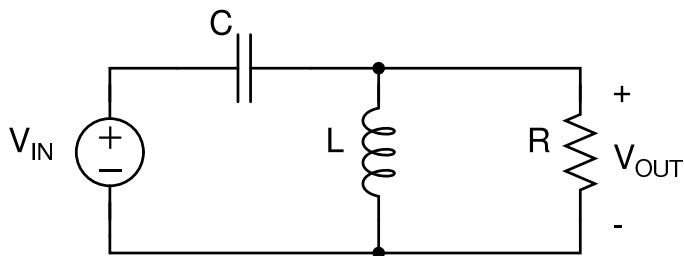
Final - EE42/100, Summer 2010 - Solutions  
August 23, 2010

1. (10 points) Consider the 2 RLC circuits below. For each circuit, assume that  $V_{IN}$  is an AC signal with angular frequency  $\omega$  (i.e.  $V_{IN} = \cos(\omega t)$ ), and sinusoidal steady-state has been achieved. Compute the transfer function of each circuit. Which one resembles a low-pass filter, and which one a high-pass filter? Be sure to mathematically justify your answers.

RLC circuit 1



RLC circuit 2



For RLC circuit 1:

$$\begin{aligned}
 V_{OUT} &= \frac{\frac{1}{j\omega C + \frac{1}{R}}}{\frac{1}{j\omega C + \frac{1}{R}} + j\omega L} \\
 &= \frac{1}{1 + j\omega \frac{L}{R} - \omega^2 LC}
 \end{aligned}$$

The magnitude is:

$$|V_{OUT}| = \frac{1}{\sqrt{(1 - \omega^2 LC)^2 + (\omega \frac{L}{R})^2}}$$

When  $\omega = 0$ ,  $|V_{OUT}| = 1$ . As  $\omega$  increases towards infinity,  $|V_{OUT}|$  approaches zero. Hence, this is a **Low-Pass filter**.

For RLC circuit 2:

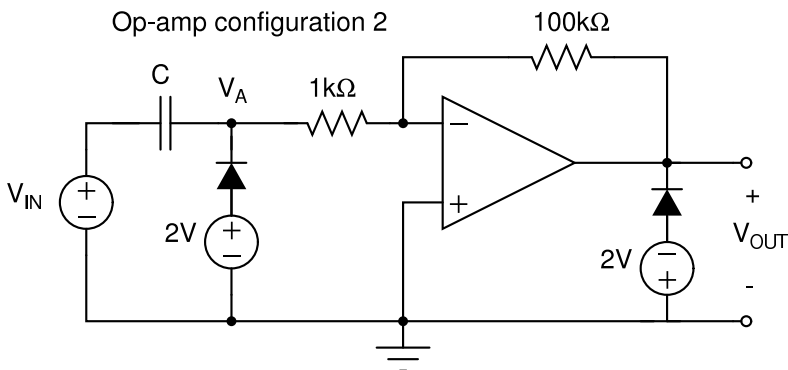
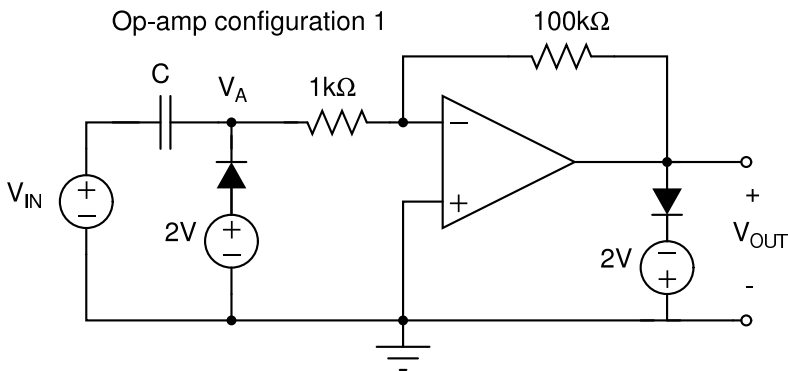
$$\begin{aligned}V_{OUT} &= \frac{\frac{1}{j\omega L + R}}{\frac{1}{j\omega L + R} + \frac{1}{j\omega C}} \\&= \frac{1}{1 + \frac{-j}{\omega L} \left( \frac{-j}{\omega C} + \frac{1}{R} \right)} \\&= \frac{1}{1 - \frac{1}{\omega^2 LC} - j \frac{1}{\omega RL}} \\&= \frac{\omega^2}{\omega^2 - \frac{1}{LC} - j \frac{\omega}{RL}}\end{aligned}$$

The magnitude is:

$$|V_{OUT}| = \frac{\omega^2}{\sqrt{\left(\omega^2 - \frac{1}{LC}\right)^2 + \left(\frac{\omega}{RL}\right)^2}}$$

When  $\omega = 0$ ,  $|V_{OUT}| = 0$ . As  $\omega$  increases towards infinity,  $|V_{OUT}|$  approaches one. Hence, this is a **High-Pass filter**.

2. (15 points) Consider the 2 diode and ideal op-amp circuits below. For each circuit, assume that  $V_{IN}$  is an AC signal ranging from  $-3$  to  $3$ . Assume also that the initial voltage across the capacitor is  $0$ , and  $C$  is large such that it doesn't discharge appreciably across one input cycle. What are the minimum and maximum values of  $V_{OUT}$  for each circuit?



For Op-amp configuration 1:

Suppose first that we disregard all circuit components to the right of  $V_A$ . The minimum voltage for  $V_A$  is  $2V$ , since if  $V_A$  tries to go below  $2V$ , the diode connecting  $V_A$  is forward-biased and shorts. The short forces  $V_A$  to become  $2V$ . When  $V_A$  is at its minimum of  $-3V$ , the maximum voltage of  $5V$  is stored across capacitor  $C$ . When  $V_A$  increases to  $3V$ , the  $5V$  across capacitor  $C$  causes  $V_A$  to increase to  $8V$ .

Meanwhile, the voltage  $V_{OUT} = -\frac{100k\Omega}{1k\Omega}V_A$ , and without the diode connecting  $V_{OUT}$ , the  $V_{OUT}$  would range from  $-200V$  to  $-800V$ . The diode connecting  $V_{OUT}$  with the  $2V$  source only ensures that  $V_{OUT}$  does not exceed  $-2V$ , so  $V_{OUT}$  is free to go from  $-200V$  to  $-800V$ .

**Maximum  $V_{OUT}$ :**  $-200V$

**Minimum  $V_{OUT}$ :**  $-800V$

For Op-amp configuration 2:

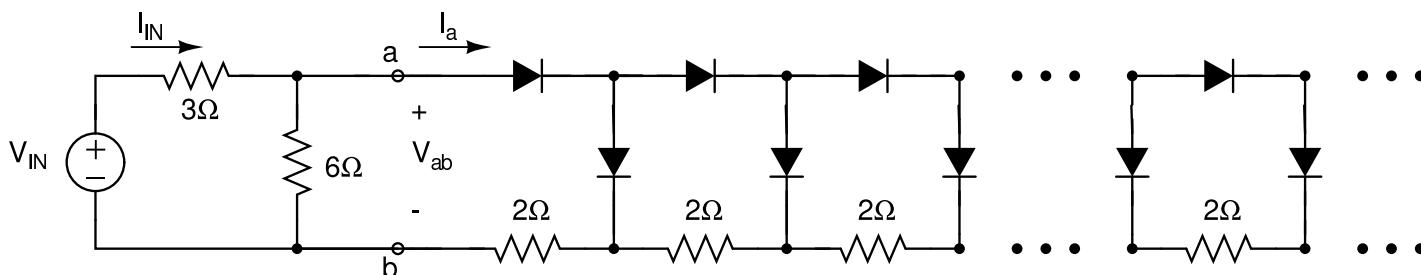
As in Op-amp configuration 1, if we first disregard all circuit components to the right of  $V_A$ , the minimum and maximum voltages for  $V_A$  would be  $2V$  and  $8V$  respectively.

Meanwhile,  $V_{OUT}$  would like to range from  $-200V$  to  $-800V$ . However, the diode and  $2V$  source connected to  $V_{OUT}$  ensures that if  $V_{OUT}$  were to ever go below  $-2V$ , the diode shorts, and  $V_{OUT}$  becomes  $-2V$ . Hence, where as  $V_{OUT}$  would go from  $-200V$  to  $-800V$  without the diode and voltage source connected to it,  $V_{OUT}$  is held at  $-2V$  with the diode and voltage source.

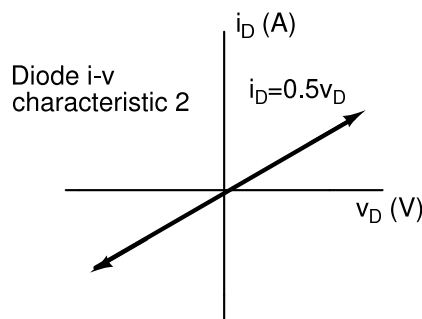
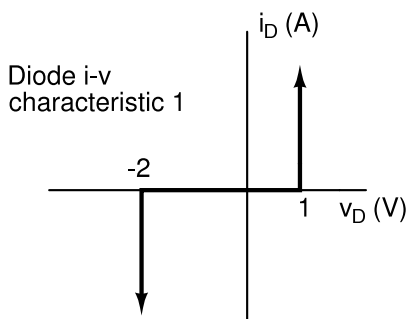
**Maximum  $V_{OUT}$ :**  $-2V$

**Minimum  $V_{OUT}$ :**  $-2V$

3. (20 points) Consider the circuit below, where an infinite diode-resistor circuit is attached to terminal  $a - b$ .



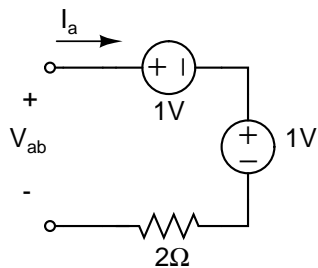
- (a) Assume that  $V_{IN} = 9V$ . Calculate the current  $I_{IN}$ , assuming that all diodes have i-v characteristic 1. Repeat for i-v characteristic 2. Use the back of this sheet if you need additional space.



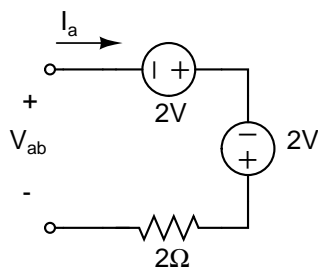
For diode i-v characteristic 1:

Consider the i-v relationship of  $I_a$  and  $V_{ab}$ . From  $-4V \leq V_{ab} < 2V$ ,  $I_a = 0$ . This is because there are a minimum of 2 diodes between terminals  $a$  and  $b$ , and for  $V_{ab} > 0$ , each diode must have a  $1V$  drop associated with it, and for  $V_{ab} < 0$ , each diode must have a  $-2V$  drop associated with it. When  $V_{ab} > 2V$ , The two diodes on the first rung of the ladder turn on, each having a  $1V$  drop. The current flowing from the bottom node of the first rung (the node that connects the diode and two resistors, which we'll denote as  $V_1$ ) to terminal  $b$  (which we'll designate as  $I_b$ ) is the same as  $I_a$ , since the current flowing into the ladder must equal the current flowing out of the ladder. Hence, we have  $I_b = I_a$ .

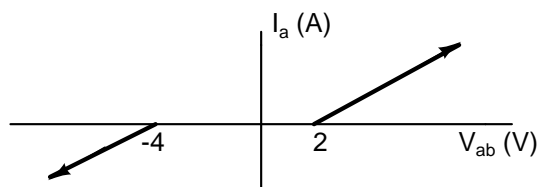
Now, for  $V_{ab} > 2V$ ,  $I_a = I_b = \frac{V_1 - V_b}{2\omega}$ , and  $V_1 = V_a - 1V - 1V$ . Hence, the only relevant components/values of the circuit that determines  $I_a$  is  $V_{ab}$ , the two diodes of the first rung, and the  $2\Omega$  resistor of the first rung, and the equivalent circuit for when  $V_{ab} > 2V$  is shown in the figure below.



A similar analysis can be applied for  $V_{ab} < -4V$ , and its equivalent circuit is shown in the figure below.



These two equivalent circuits give us the following i-v relationship between  $V_{ab}$  and  $I_a$ :

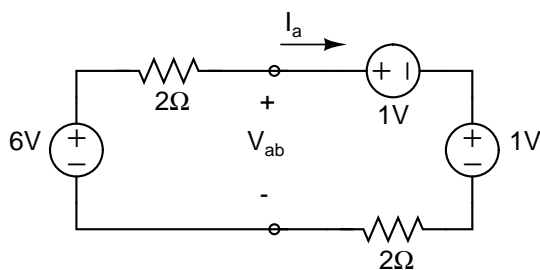


Taking the Thevenin equivalent of the circuit to the left of terminal a-b, with  $V_{IN} = 9V$ , we have:

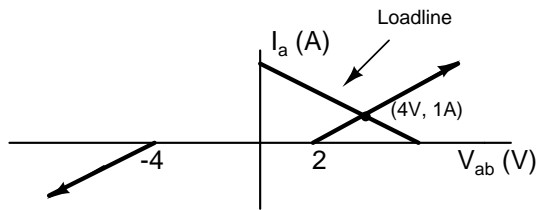
$$V_{th} = \frac{6\Omega}{6\Omega + 3\Omega} V_{IN} = \frac{2}{3} 9V = 6V$$

$$R_{th} = \frac{1}{\frac{1}{3\Omega} + \frac{1}{6\Omega}} = 2\Omega$$

Because  $V_{th} > 0$ , we only need to worry about the case where  $V_{ab} > 0$ . The equivalent circuit is:



The figure below plots the loadline from the Thevenin equivalent circuit, along with the i-v relationship between  $V_{ab}$  and  $I_a$ .



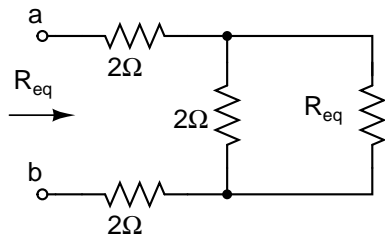
The intersection between the loadline and the i-v relationship is at  $V_{ab} = 4V$  and  $I_a = 1A$ . Hence, we have  $V_{ab} = 4V$ , and

$$I_{IN} = I_a + \frac{V_{ab}}{6\Omega} = 1A + \frac{4V}{6\Omega}$$

$$I_{IN} = 1.67A$$

For diode i-v characteristic 2:

This i-v characteristic is the same as that of a  $2\Omega$  resistor, and hence, we have an infinite ladder of resistors. We must compute the equivalent resistance  $R_{eq}$  of the ladder, noting that adding an additional rung to the ladder does not change the equivalent resistance since the ladder is infinite. With this in mind, the following figure shows the equivalent circuit:



From this circuit, we get that:

$$R_{eq} = 2 + 2 || R_{eq} + 2$$

$$R_{eq} = 4 + \frac{1}{\frac{1}{2} + \frac{1}{R_{eq}}}$$

$$R_{eq} = 4 + \frac{R_{eq}}{\frac{R_{eq}}{2} + 1}$$

$$\frac{1}{2}R_{eq}^2 + R_{eq} = 2R_{eq} + 4 + R_{eq}$$

$$0 = R_{eq}^2 - 4R_{eq} - 8$$

Solving, we get  $R_{eq} = 2(1 + \sqrt{3}) = 5.4641\Omega$ .

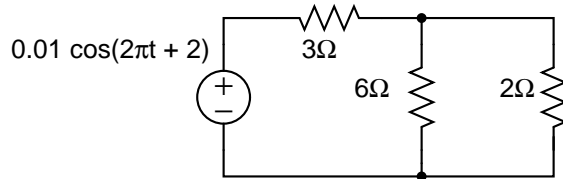
Solving for  $I_{IN}$ , we have  $I_{IN} = \frac{V_{IN}}{3 + \frac{1}{\frac{1}{6} + \frac{1}{5.4641}}} A = 1.5359A$



- (b) Assume that  $V_{IN}$  is now corrupted with an AC noise signal, such that  $V_{IN} = 0.01\cos(2\pi t + 2) + 9V$ . You may assume the AC component is small enough such that from its perspective, all relevant circuit components appear linear. Repeat part (a) using this new  $V_{IN}$  using ONLY diode i-v characteristic 1.

For diode i-v characteristic 1, at  $V_{IN} = 9V$ , the Q-point of infinite resistor-diode ladder, according to part (a), is  $(V_{abQ}, I_{aQ}) = (4V, 1A)$ . At this Q-point, the i-v characteristic of the ladder (relationship between  $V_{ab}$  and  $I_a$ ) is linear with a slope of 0.5. Hence, the small signal resistance of the ladder,  $r_D$ , is  $r_D = \frac{\Delta V_{ab}}{\Delta I_a} = 2\Omega$ .

The equivalent small-signal equivalent circuit is then:



The small AC signal component of  $I_{IN}$  is therefore:

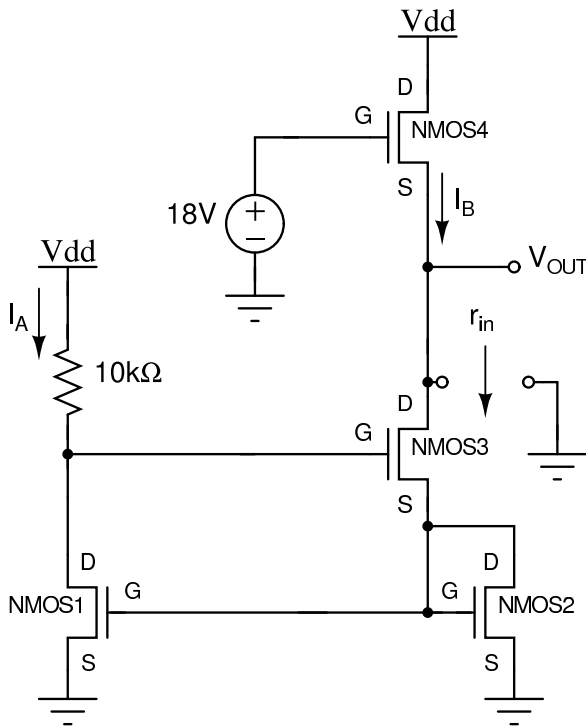
$$\begin{aligned} I_{IN,ac} &= \frac{0.01 \cos(2\pi t + 2)}{3 + \frac{1}{\frac{1}{6} + \frac{1}{2}}} \\ &= \frac{2}{9} * 0.01 \cos(2\pi t + 2) \end{aligned}$$

The DC signal component,  $I_{IN,dc}$ , is computed in part (a), and determined to be 1.67A.

The overall current is then  $I_{IN} = I_{IN,ac} + I_{IN,dc} = \frac{2}{9} * 0.01 \cos(2\pi t + 2) + 1.67A$ .

4. (15 points) Consider the 4-NMOS circuit in the figure below. Assume that  $V_{dd} = 20V$ , and for all NMOS transistors,  $K = 0.25mA/V^2$  and  $V_{to} = 3V$ .

(a) Assume that all NMOS's are in saturation mode. Find  $I_A$  and  $I_B$ .



Assuming that all NMOS's are in saturation mode, we begin by noting that the gate-to-source voltage,  $V_{GS}$ , for NMOS1 is the same as  $V_{GS}$  for NMOS2. Because the same ( $I_B$ ) current flows through NMOS2, NMOS3, and NMOS4, we have that all NMOS's have the same  $V_{GS}$ .

To compute  $I_A$ , we can set up a KVL equation involving the  $V_{GS}$  voltages of NMOS1 and NMOS3:

$$\begin{aligned} -V_{dd} + 10000I_A + 2V_{GS} &= 0 \\ 10 &= 5000I_A + V_{GS} \end{aligned}$$

This gives us the loadline equation for NMOS1 involving  $V_{GS}$  and  $I_A$ . The saturation-mode equation is  $I_A = 0.25(V_{GS} - 3)^2$ , and the intersection of the saturation-mode equation with the loadline equation occurs when  $V_{GS} = 5V$ , and  $I_A = 1mA$ .

Hence, we have that  $I_A = I_B = 1mA$ .

- (b) Note that part (b) refers to the same circuit as in part (a). Find  $V_{OUT}$ , and verify that all NMOS transistors are in saturation mode.

Denote  $V_{DS1}$  as the drain-to-source voltage for NMOS1,  $V_{DS2}$  as the drain-to-source voltage for NMOS2,  $V_{DS3}$  as the drain-to-source voltage for NMOS3, and  $V_{DS4}$  as the drain-to-source voltage for NMOS4.

For NMOS1:

$$\begin{aligned}V_{DS1} &= V_{dd} - 10000I_A = 20 - 10000 * 0.001 = 10V \\V_{DS1} &> V_{GS} - V_{to} = 5 - 3 = 2V\end{aligned}$$

For NMOS2:

Note that  $V_{DS2} = V_{GS}$ . We have:

$$V_{DS2} = 5V > V_{GS} - V_{to} = 5 - 3 = 2V$$

For NMOS3:

Note that  $V_{OUT} = 18 - V_{GS} = 18 - 5 = 13V$ .

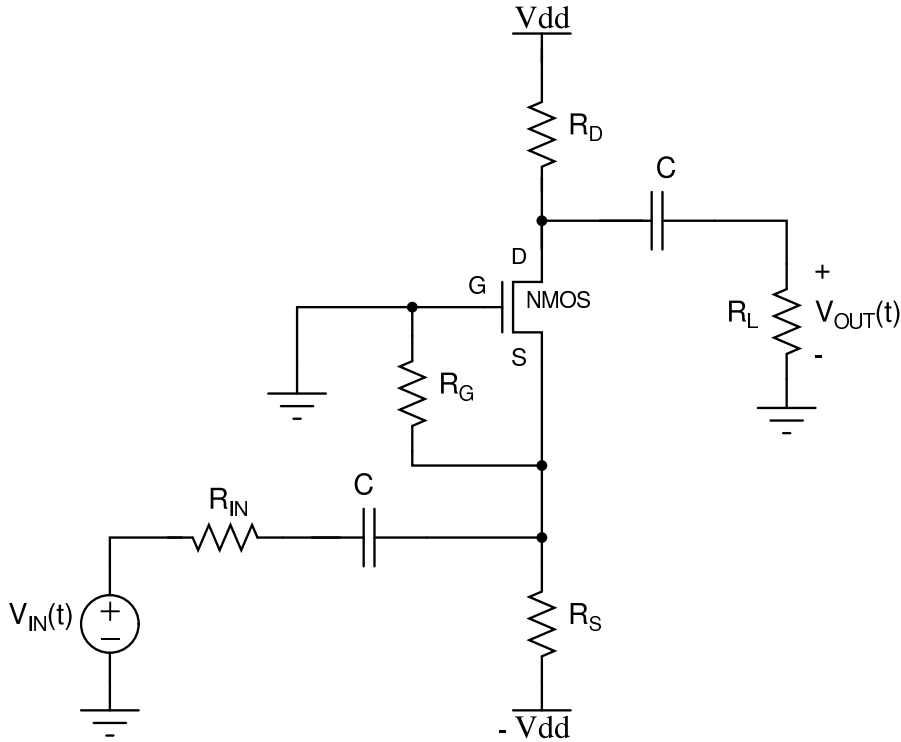
$$V_{DS3} = 13 - 5 = 8V > V_{GS} - V_{to} = 5 - 3 = 2V$$

For NMOS4:

$$V_{DS4} = 20 - 13 = 7V > V_{GS} - V_{to} = 5 - 3 = 2V$$

Hence, the drain-to-source voltage of all NMOS's are greater than the difference between their gate-to-source voltages and their threshold voltages, implying that all NMOS's are in saturation. We've also calculated that  $V_{OUT} = 13V$ .

5. (20 points) Consider the following NMOS circuit. Assume that  $V_{IN}(t)$  is a small AC signal, and that the NMOS is in saturation mode.



- (a) Write three equations that allow you to solve for the three DC Q-point voltages/currents: the voltage from gate (G) to source (S), the voltage from drain (D) to source (S), and the current from drain to source. What is the transconductance?

Denote the current through resistor  $R_G$  as  $I_G$ . Doing KVL from the drain to source of the NMOS, we have:

$$-V_{dd} + I_D R_D + V_{DS} + (I_D + I_G) R_S - v_{dd} = 0 \quad (1)$$

Doing KVL from the gate to source of the NMOS we have:

$$V_{GS} + (I_D + I_G) R_S - V_{dd} = 0 \quad (2)$$

Lastly, we can relate  $I_G$  and  $R_G$  by:

$$I_G = \frac{V_{GS}}{R_G} \quad (3)$$

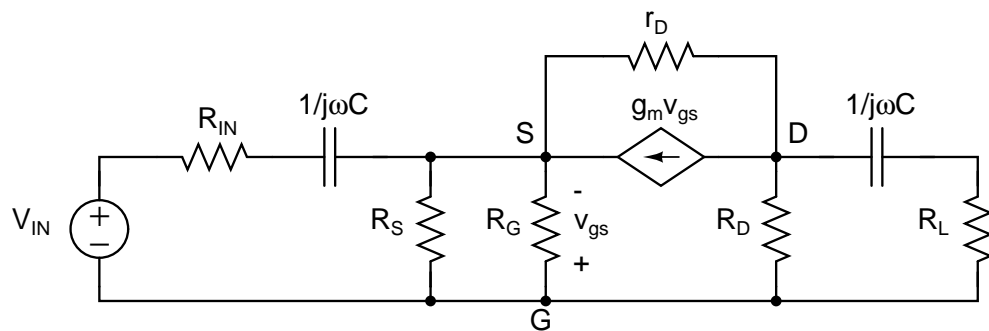
Substituting equation 3 into equations 1 and 2, and adding the equation that relates  $I_D$  and  $V_{GS}$  for saturation mode of the NMOS, we have the following three equations:

$$2V_{dd} = I_D(R_D + R_S) + V_{GS} \frac{R_S}{R_G} + V_{DS}$$

$$I_D = K(V_{GS} - V_{to})^2$$

$$V_{dd} = V_{GS} \left(1 + \frac{R_S}{R_G}\right) + I_D R_S$$

- (b) Assume that for the circuit in part (a), the capacitances are NOT very large, such that they do NOT appear as a short-circuit to AC signals. Draw the small-signal equivalent circuit, assuming that  $V_{IN}(t) = 0.05\cos(\omega t + 2)$  and sinusoidal steady-state has been achieved.



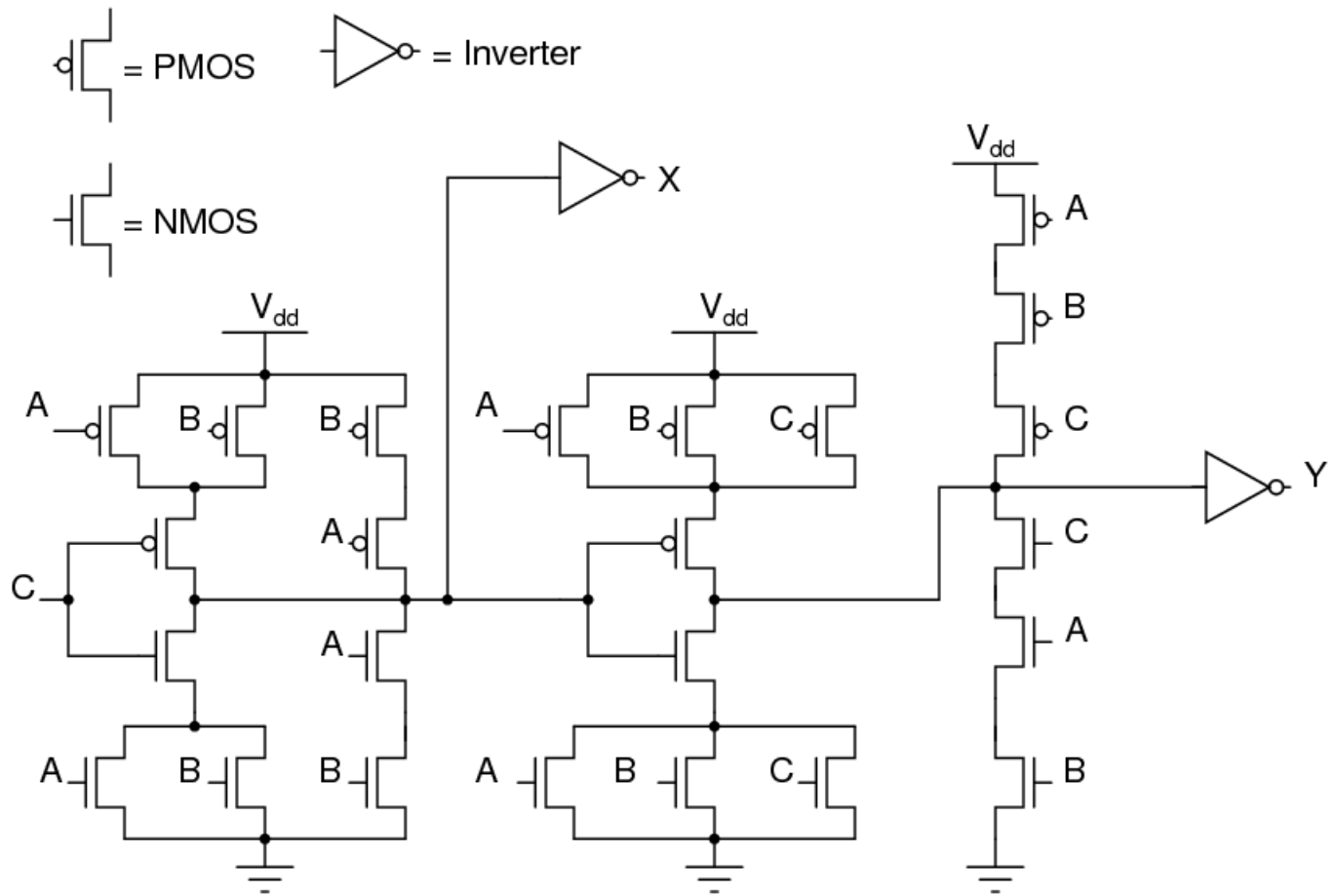
Note:  $r_D$  does not need to be shown in the circuit diagram.

- (c) Demonstrate how you would solve for  $V_{OUT}(t)$ . You don't have to explicitly solve for  $V_{OUT}(t)$ , but you should set up a set of equations and write brief explanations to show how  $V_{OUT}(t)$  can be obtained in terms of the transconductance  $g_m$  and values of all circuit components.

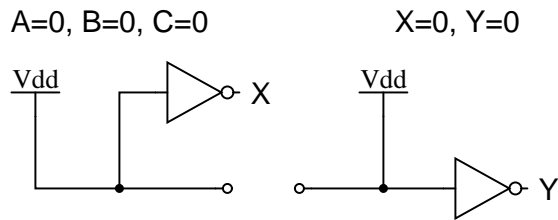
Do node-voltage or mesh-current analysis using phasors by setting up KVL/KCL equations. Details omitted here.

6. (20 points) Consider the CMOS logic circuit (with 24 NMOS/PMOS components) in the figure below, where the NMOS, PMOS, and inverter symbols are denoted. The inputs are  $A$ ,  $B$ , and  $C$ , while the outputs are  $X$ , and  $Y$ .

- (a) Find the truth table for the 3 inputs and 2 outputs. Note that inputs  $A$ ,  $B$  are symmetric in their implementation (i.e. the input  $(A, B, C) = (0, 1, 1)$  should give the same outputs as the input  $(A, B, C) = (1, 0, 1)$ ). You will be graded generously on this problem.
- (b) For a BONUS of 2 points, determine what purpose this CMOS circuit serves based off of your truth table.

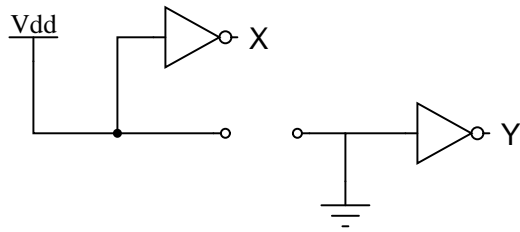


The following are the set of distinct equivalent circuits:



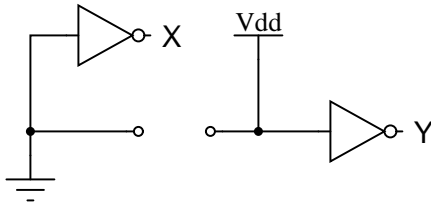
A=0, B=0, C=1

X=0, Y=1



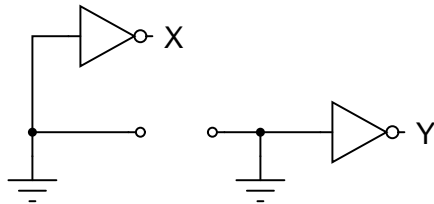
A=0, B=1, C=1

X=1, Y=0



A=1, B=1, C=1

X=1, Y=1



Note that the circuits for  $A = 0, B = 1, C = 0$  and  $A = 1, B = 0, C = 0$  are the same as for  $A = 0, B = 0, C = 1$ . The circuits for  $A = 1, B = 0, C = 1$  and  $A = 1, B = 1, C = 0$  are the same as for  $A = 0, B = 1, C = 1$ .

Based on these circuits, the truth table is the following:

A	B	C	X	Y
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This truth table is the same as that of a **Full Adder**, whereby  $A$  and  $B$  are the binary values to be added,  $C$  is the carry-in bit,  $X$  is the carry-out bit, and  $Y$  is the result of the binary addition (excluding the carry-out bit).